

10HZ PULSED POWER CONVERTERS FOR THE ISIS SECOND TARGET STATION (TS-2)

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Abstract

The Extracted Proton Beamline to the ISIS second target station has two 10Hz pulsed magnet systems which extract the proton from the existing 50Hz beamline. Kicker 1 magnet system deflects the beam 12.1mrad and Kicker 2 magnet system deflects the beam 95mrad. Both magnets are identical, however each pulsed power converter is considerably different. This paper describes the design requirements, topology, installation, testing and successful operation of both pulsed power converters.

INTRODUCTION

ISIS, Figure 1, sited at the Rutherford Appleton Laboratory (RAL) is one of the world's most intense pulsed neutron source. Intense bursts of neutrons are produced at 20mS (50Hz) intervals when a heavy metal target is bombarded by a high-energy (800MeV) proton beam from a synchrotron accelerator releasing neutrons by the process of spallation. Over the past 3 years a second target station (TS-2) has been constructed. TS-2 will provide a 10Hz beam for up to 18 new instruments. The 10Hz proton beam is achieved by operating two slow pulsed magnets and a septum magnet to direct the proton beam to TS-2 Extract Proton Beam line (EPB). The TS-2 EPB, 149 metres long, will require 56 magnets and their associated power supplies to produce magnetic fields for the beam optics. The power supply ratings range from 1.5kW to 160kW with one 680kW DC septum power supply and the two 10Hz pulsed power supplies.

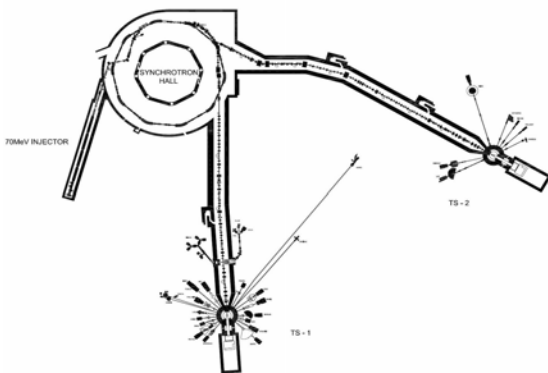


Figure 1: ISIS Layout.

10HZ PULSED POWER CONVERTERS

The pulsed power converters and the kicker magnets (the same magnet design was used for each kicker system) were designed and manufactured by Danfysik AS

in Denmark. They provide a half sine wave current profile with a 12mS rise time, 600µS flat top and a 12mS fall time. The 600µS flat top will give 100ppm field stability within each of the kicker magnets. Each power converter is based on a high voltage capacitor bank to drive up the current to the required level (319A Kicker 1 and 2556A Kicker 2) and a low voltage capacitor bank to achieve the flat top requirement for a minimum of 600µS. The stored energy in the magnet is recovered back into the high voltage capacitor bank to reduce the power requirements.

PSU Type	Power (kW)	Maximum Voltage (V)	Maximum Current (A)
K1 12.1mrad	2	235	450
K2 90mrad	30	1355	2800

Table 1: 10Hz Pulsed Power Converter Maximum Ratings.

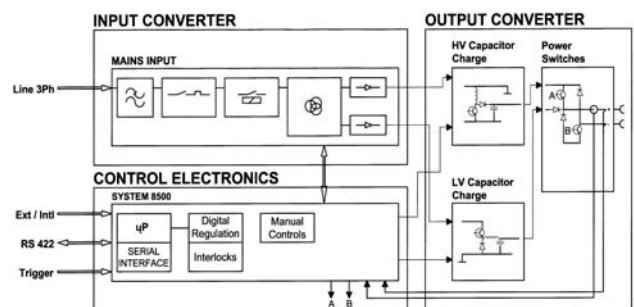


Figure 2: Block diagram of 10Hz Pulsed Power Converter.

Input Converter.

The AC main input supply is EMI filtered and over current protected with a manually operated circuit breaker. There is two stage switching to minimise the inrush current. A three phase transformer (Delta input, star/delta output) converts the mains voltage to a lower level and provides galvanic isolation.

The transformer output voltage is rectified in a twelve pulse rectifier and filtered with a L-C low pass filter to produce a dc link voltage for the output converter.

Output Converter.

The output converter consists of three major blocks. A high voltage capacitor pre-charger, a low voltage capacitor pre-charger and the power output switches IGBT A and IGBT B (see Figure 2).

Switch Control Principle.

When the capacitors are charged to their specific value, a ready signal is generated and sent to the regulation loop. A trigger signal from ISIS will then start the 10Hz pulse sequence. IGBT A and IGBT B are turned on. The flat top period begins after the digitally controlled output current reaches the desired set value, which is 319A for kicker 1 and 2556A for kicker 2. IGBT A is then turned off and IGBT B will continue to carry the output current. Figure 3 shows the measured half sine wave current pulses for the kickers. Figure 4 shows the kicker output voltage wave.

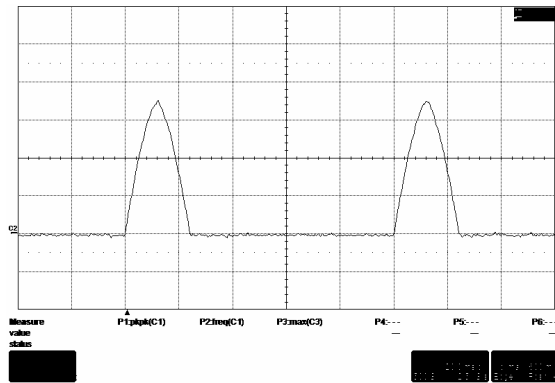


Figure 3: Kicker Measured 10Hz pulse.

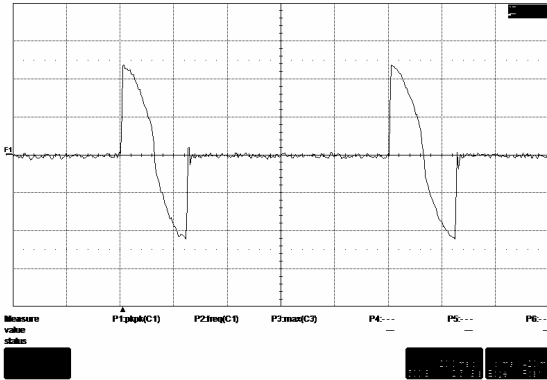


Figure 4: Kicker Measured output voltage.

The flat top for kicker 1 and slope-top for kicker 2 is digitally loop controlled with a duration of a minimum of 600µS (see figure 5 and figure 6). IGBT B will then open starting the recovery period. In the recovery period the current will flow back to the HV capacitor through its top diode. As soon as IGBT B is opened the capacitor will also start to re-charge ready for the next pulse.

On Kicker 1 a measure of the flat top accuracy is achieved from the following principle:

$$\text{dc flat top voltage} = \text{resistive load} \times \text{current.}$$

Then the voltage across the load inductor will be zero. No voltage across the inductor is an indication of no change of current.

On kicker 2 to maintain the 100ppm field in the magnet it was realized that instead of a flattop we had to

introduce a small slope into the wave shape. The slope-top wave shape is maintained by sampling the current value at the beginning and at the end of the flattop. Based on the difference between the two measurements, the LV capacitor bank voltage (which affects the slope) is adjusting accordingly. The Regulation Module has the option to maintain a specified slope-top instead of a flattop. The slope is now a function of the current

$$\text{slope} = a * \text{Iset} + b$$

instead of a constant as on kicker 1.

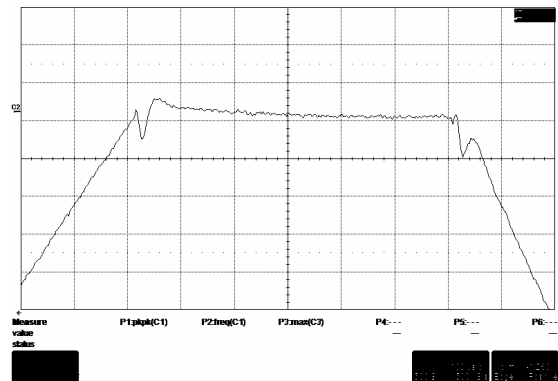


Figure 5: Kicker 1 Measured 10Hz flat top.

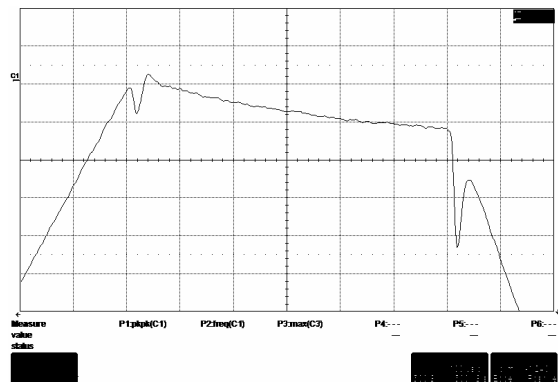


Figure 6: Kicker 2 Measured 10Hz Slope-top.

High Voltage Capacitor Charger.

The high voltage capacitor charger is a boost converter boosting the dc link voltage to a value between 50 and 100% of nominal value set by the regulation module. The boost converter is based on the Danfysik 859 series building blocks. The 859 converter is a current mode switch regulator suitable for charging larger capacitor loads. The voltage regulation is manufactured to an accuracy of 0.25% thus ensuring a flat top jitter of better than ±60µS. The control module has light guides for input and output. The input light guide is a PWM modulated signal with a fixed frequency noting the charge voltage level. A missing pulse disables the charging converter.

The output light guide has three indication states:

- Continuous off. (module fault, IGBT fault or over load)
- Pulses. (charging in progress)
- Continuous on. (capacitor voltage within specification and ready to be fired)

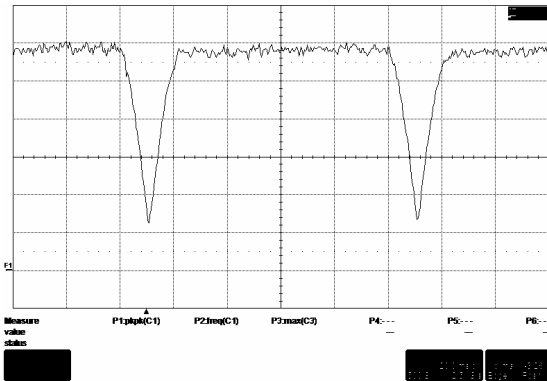


Figure 7: Kicker High voltage capacitor voltage waveform.

Fig 8 to be added

Figure 8: Kicker High voltage capacitor current waveform.

Low Voltage Capacitor Charger.

The low voltage capacitor charger is a buck converter controlling the dc link voltage to a value equal to the required voltage at flat top. This is a level voltage given by the regulation module. This voltage is constantly adjusted by the digital loop to an accuracy of 1%. This equals a flat top deviation of better than 100ppm.

The control module for the LV capacitor charger works on the same principle as the HV capacitor charger.

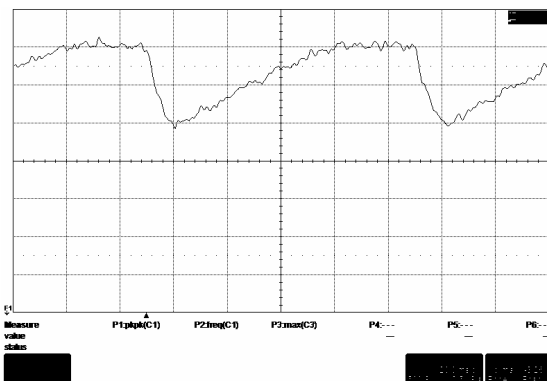


Figure 11: Kicker Low voltage capacitor voltage waveform.

Fig 12 to be added

Figure 12: Kicker Low voltage capacitor current waveform.

Control Electronics.

The control electronics has to perform the following tasks:-

- Control of the input converter block.
- Control of the output converter block

- Communication. Remote & Local
- Current measurement and regulation control
- Status and monitoring.
- Interlocks. Internal & external.

Installation.

The kicker power converters were installed into the Isis R6 power supply hall in August 2007. They were first run in November 2007. A proton beam was successfully extracted using the kicker power converters on 14 December 2007.

Output Cables.

As the kicker 2 pulse is running at a level of 2556A the forces on the output cables are considerable. The standard idea of running two single core cables close together would give us an inductance of 0.46uH/m and a force of 74N/m (8kg/m). We decided on using a 4-core armoured cable with the positive and negative cables being diagonally opposite each other to reduce forces (see figure 13). Whilst the inductance increased to 0.615uH/m (33% higher than the two single core cables) the forces were greatly reduced to 12.4N/m (1.35kg/m).

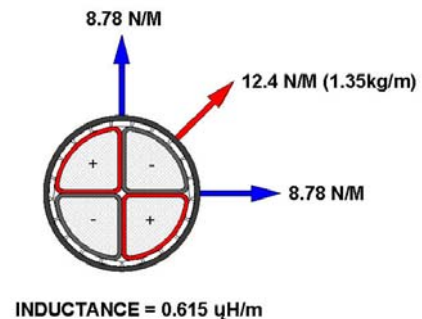


Fig 13 Output cable profile.

ACKNOWLEDGMENTS

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